REMARKS

It is believed that the above amendments and following remarks attend to each and every rejection and objection presented in the pending September 21, 2005 office action. Claims 1-29 remain pending, with claims 1, 10, 16 and 23 being independent. Claims 4, 5, 13, 19 and 26 are amended for clarification of the acronym 'HLSN' without adding new matter.

Specification

As required by paragraph 2 of the pending office action, paragraph [0001] is amended to insert information of related applications. Reconsideration is requested.

Claim Rejections – 35 U.S.C. §102

Claims 1-29 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Publication No. US 2003/0237067 A1 to Mielke et al. (hereinafter "Mielke"). Respectfully, we disagree.

As way of background, the following summary may help clarify the differences between the immediate application and Mielke. The immediate application teaches a method and system for performing circuit analysis on a circuit design. Instantiation paths for one or more design blocks of the circuit design are determined and select information is recursively accumulated for each of the design blocks. Instantiation characteristics are applied to the accumulated information for each instance of the design blocks based upon instantiation hierarchy of the instance within the circuit design. Thus, select information for each design block is recursively summed only once, no matter how many times it is instantiated within the circuit design. See at least paragraph [0039] of the immediate application.

On the other hand, Mielke discloses a system and method for automating a static-timing analysis of an integrated circuit design. Mielke is concerned with automating the process of analyzing an integrated circuit design and does not disclose a particular analysis method. In paragraph [0011], Mielke discloses that "the process adapts to collect and format information used to simulate functional blocks within an integrated circuit design in response to interchangeable and selectable timing models" and that "timing models reduce complexity of the integrated circuit representation by

removing arcs from the design." Notably, Mielke does not disclose accumulating select information of design blocks or applying instantiation characteristics to the accumulated information. Mielke is clearly different from the claims of the immediate application.

In particular, to anticipate a claim, Mielke must teach every element of the claim and "the identical invention must be shown in as complete detail as contained in the ... claim." MPEP 2131 citing Verdegaal Bros. V. Union Oil Co. of California, 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987) and Richardson v. Suzuki Motor Co., 868 F.2d 1226, 9 USPQ2d 1913 (Fed. Cir. 1989). Mielke does not teach every element of claims 1-29.

Claim 1 recites a method for performing circuit analysis on a circuit design, including:

a) determining instantiation paths for one or more design blocks of the circuit design;

b) recursively accumulating select information for each of the design blocks; and

c) applying instantiation characteristics to the accumulated information for each instance of the design blocks based upon instantiation hierarchy of the instance within the circuit design.

Step a) of claim 1 requires that instantiation paths for one or more design blocks of the circuit design are determined. As taught by paragraph [0031] of the immediate application, instantiation paths for one or more design blocks are for example determined from instantiation hierarchy 134' by analysis tools 120. As shown by the example of FIGs. 5, 6 and 7, design block D is instantiated within design block C, which is instantiated within design block A and within design block B. Since design block B is also instantiated within design block A, design block D is determined to have instantiation paths A1.C1.D1 and A1.B1.C2.D2, as shown in table 130 of FIG. 8.

Mielke, however, does not disclose determining instantiation paths for one or more design blocks as required by step a).

Step b) of claim 1 requires that select information is recursively accumulated for each of the design blocks. As for example taught by paragraph [0032] of the immediate application, analysis tool 120 sums select, common information of design elements and signal nets of design blocks A-E. Specifically, for each design block, analysis tool 120 recursively traverses circuit design 116 to sum select information of the design block and all included design blocks.

Mielke, on the other hand, does not disclose recursively accumulating select information for each of the design blocks. In fact, teaching away from step b), Mielke recites "the plurality of data files are used to formulate a hierarchically arranged model of the various signal paths that associate the various functional blocks of the integrated circuit design." See Mielke, paragraph [0066]. Clearly, the model of Mielke is not based upon select recursively-accumulated values of each design block.

Step c) of claim 1 requires that instantiation characteristics be applied to the accumulated information of step b) for each instance of the design blocks based upon instantiation hierarchy of the instance within the circuit design. Since Mielke does not recursively-accumulate select values, Mielke cannot apply instantiation characteristics to the values. For at lease these reasons, Mielke cannot anticipate claim 1.

Reconsideration of claim 1 is respectfully requested.

Claims 2-9 depend from claim 1 and benefit from like argument. However, these claims have additional features that patentably distinguish over Mielke. For example, claim 2 recites that the select information includes one or more of FET capacitance, FET width and wire capacitance. Mielke does not disclose recursively accumulating any of FET capacitance, FET width and wire capacitance.

Claim 3 recites that the instantiation characteristics include one or more of switching frequencies and scaling factors. Mielke does not disclose or suggest applying one or more of switching frequencies and scaling factors to the recursively-accumulated information.

Claim 4 recites recursively accumulating selected information for one or more highest level signal name (HLSN) signal nets within the design blocks. Mielke does not recursively accumulate selected information for one or more HLSN signal nets within the design blocks.

Claim 5 recites selecting the one or more highest level signal names (HLSNs) through a user interface. Claim 6 recites selecting the one or more blocks through a user interface. Mielke's user interface disclosed in paragraphs [0027-29] does not disclose or suggest that the user interface is usable for selecting blocks and HLSNs.

Claim 7 recites reading instantiation hierarchy from the circuit design to determine the instantiation paths. Since, as argued above, Mielke does not determine instantiation paths, Mielke has no need to read instantiation hierarchy from the circuit design.

Claim 8 recites reading instantiation characteristics from the circuit design. Claim 9 recites generating results based upon applied instantiation characteristics. Since, as argued above, Mielke does not apply instantiation characteristics to recursively accumulated values, Mielke cannot generate results based upon instantiation characteristics and recursively accumulated values.

For at least these reasons, Mielke cannot anticipate claims 2-9. Reconsideration of claim 2-9 is respectfully requested.

Claim 10 recites a system for performing circuit analysis on a circuit design, including:

a) a user interface for selecting one or more design blocks of the circuit design;

b) an analysis tool operable to determine instantiation paths for the design blocks, accumulate select information for each instance of each of the design blocks, and apply instantiation characteristics of each instance to the accumulated information; and

c) memory for storing the instantiation paths, the accumulated information, and results based upon the applied characteristics.

Mielke's user interface is used to select a static-timing engine (see, e.g., Mielke paragraphs [0063] and [0068]); but Mielke does not disclose using the user interface to select one or more design blocks of the circuit design as required by element a) of claim 10. Mielke further does not disclose an analysis tool operable to determine instantiation paths for design blocks, accumulate select information for

each instance of each of the design blocks, or apply instantiation characteristics of each instance to the accumulated information, as required by step b) of claim 10. Since Mielke does not disclose step b), Mielke also cannot disclose step c), which requires that memory store the instantiated paths, the accumulated information and results based upon the applied characteristics.

For at least these reasons, Mielke cannot anticipate claim 10. Reconsideration of claim 10 is respectfully requested.

Claim 11-15 depend from claim 10 and benefit from like argument. These claims, however, have additional features that patentably distinguish over Mielke. For example, claim 11 recites that the select information includes one or more of FET capacitance, FET width and wire capacitance. Again, Mielke does not recursively accumulate select information and therefore cannot disclose select information including one or more of FET capacitance, FET width and wire capacitance. Claim 12 recites that the instantiation characteristics include one or more of switching frequencies and scaling factors. Mielke does not disclose – anywhere – switching frequencies or scaling factors. Claim 13 recites that the analysis tool is operable to recursively accumulate the select information for one or more highest level signal name (HLSN) signal nets within the design blocks. Again, Mielke does not disclose recursively accumulating select information, nor recursively accumulating select information for one or more HLSNs. Claim 14 recites that the analysis tool is operable to read an instantiation hierarchy of the circuit design to determine the instantiation paths. As argued above, Mielke does not determine instantiation paths. Claim 15 recites that the analysis tool is operable to read the instantiation characteristics from the circuit design. Mielke does not teach or suggest instantiation characteristics nor reading such characteristics from the circuit design.

For at least these reason, Mielke cannot anticipate claims 11-15. Reconsideration of claims 11-15 is respectfully requested.

Claim 16 recites a system for performing circuit analysis on a circuit design, including:

a) means for determining instantiation paths for one or more design blocks of the circuit design;

b) means for recursively accumulating select information for each of the design blocks; and

c) means for applying instantiation characteristics to the accumulated information for each instance of the design blocks based upon instantiation hierarchy of the instance within the circuit design.

Among other differences, Mielke does not determine instantiation paths for one or more design blocks of the circuit design, as required by element a) of claim 16. Mielke also does not recursively accumulate select information for each design block, as required by element b). Since Mielke does not accumulate information, Mielke also cannot apply instantiation characteristics to the accumulated information, as required by element c). For at least these reasons, Mielke cannot anticipate claim 16. Reconsideration of claim 16 is respectfully requested.

Claims 17-22 depend from claim 16 and benefit from like argument. However, these claims have additional features that patentably distinguish over Mielke. For example, claim 17 recites that the select information includes one or more of FET capacitance, FET width and wire capacitance. Mielke does not disclose – anywhere – that one or more of FET capacitance, FET width and wire capacitance is accumulated. Claim 18 recites that the instantiation characteristics include one or more of switching frequencies and scaling factors. As noted above, Mielke does not disclose applying one or more of switching frequencies and scaling factors to the accumulated values. Claim 19 recites that the means for recursively accumulating includes means for recursively accumulating select information of one or more highest level signal name (HLSN) signal nets of the design blocks. As noted above, Mielke does not disclose recursively accumulating in any capacity. Claim 20 recites means for reading instantiation hierarchy from the circuit design to determine the instantiation paths. As argued above, Mielke does not determine instantiation paths. Claim 21 recites means for reading instantiation characteristics from the circuit design; and claim 22 recites means for generating results based upon applied instantiation characteristics. Since, as argued above, Mielke does not apply instantiation characteristics, Mielke cannot generate such results.

For at least these reasons, Mielke cannot anticipate claims 17-22. Reconsideration of claims 17-22 is respectfully requested.

Claim 23 recites a software product having instructions, stored on computer-readable media, wherein the instructions, when executed by a computer, perform steps for performing circuit analysis on a circuit design, including:

a) instructions for determining instantiation paths for one or more design blocks of the circuit design;

b) instructions for recursively accumulating select information for each of the design blocks; and

c) instructions for applying instantiation characteristics to the accumulated information for each instance of the design blocks based upon instantiation hierarchy of the instance within the circuit design.

As above, Mielke does not disclose determining instantiation paths for one or more design blocks, as required by element a) of claim 23. Mielke also does not disclose recursively accumulating select information for each of the design block, as required by element b). Mielke cannot, therefore, apply instantiation characteristics to the accumulated information based upon instantiation hierarchy of the instance, as required by element c).

Therefore Mielke cannot anticipate claim 23. Reconsideration of claim 23 is respectfully requested.

Claims 24-29 depend from claim 23 and benefit from like argument. However, these claims have additional features that patentably distinguish over Mielke. For example, claim 24 recites that the select information includes one or more of FET capacitance, FET width and wire capacitance. Again, Mielke does not disclose recursively accumulating select information of FET capacitance, FET width and wire capacitance. Claim 25 recites that the instantiation characteristics include one or more of switching frequencies and scaling factors. Again, Mielke does not disclose instantiation characteristics of switching frequencies and scaling factors. Claim 26 recites that the instructions for recursively accumulating include instructions for recursively accumulating the select information for one or more highest level signal name (HLSN) signal nets within the design blocks. Again, Mielke does not disclose

recursively accumulate in any capacity. Claim 27 recites reading instantiation hierarchy from the circuit design to determine the instantiation paths. Mielke does not teach or suggest reading instantiation hierarchy from the circuit design to determine instantiations paths. Claim 28 recites reading instantiation characteristics from the circuit design. As Mielke does not apply instantiation characteristics, Mielke also does not disclose reading instantiation characteristics from the circuit design. Claim 29 recites generating results based upon applied instantiation characteristics. Mielke does not apply instantiation characteristics and therefore cannot generate results based upon applied instantiation characteristics.

For at least theses reasons, Mielke cannot anticipate claims 24-29. Reconsideration of claims 24-29 is respectfully requested.

In view of the above amendments and arguments, we ask for reconsideration of all claims and solicit a notice of allowance therefore.

It is believed that no fees are due in connection with this amendment. If any fee is due, please charge Deposit Account No. 08-2025.

Respectfully submitted,

By: 

Curtis A. Vock, Reg. No. 38,356
LATHROP & GAGE L.C.
4845 Pearl East Circle, Suite 302
Boulder, CO 80301
Telephone: (720) 931-3011
Facsimile: (720) 931-3001